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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/079,767	02/19/2002	Jens Graf	10191/2246	7845
26646	7590	01/18/2007	EXAMINER	
KENYON & KENYON LLP ONE BROADWAY NEW YORK, NY 10004			NGUYEN, THAN VINH	
			ART UNIT	PAPER NUMBER
			2187	
SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE		
3 MONTHS	01/18/2007	PAPER		

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)
	10/079,767	GRAF ET AL.
	Examiner	Art Unit
	Than Nguyen	2187

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 10/27/06.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-8 is/are pending in the application.
 - 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1-8 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 19 February 2002 is/are: a) accepted or b) objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) <input type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date: _____
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)	5) <input type="checkbox"/> Notice of Informal Patent Application
Paper No(s)/Mail Date: _____	6) <input type="checkbox"/> Other: _____

DETAILED ACTION

1. This is a response to the amendment, filed 10/27/06.
2. Claims 1-8 are pending.

Response to Amendment/Argument

3. Applicant's arguments filed 10/27/06 have been fully considered but they are not persuasive. Applicant has added new limitations to the claims. These are addressed below. The following is the Examiner's interpretation of the claims (with broadest interpretation) and how Norman meets it. In claim 1/5 Applicant claims a memory arrangement comprising and its associated method of operation: a programmable memory; a first buffer memory to store a command (input buffer 48 stores commands going toward decoder 62; Fig. 4; 6/60-65; 6/50-54), subsequent command are also stored in the buffer sequentially (data stored in the buffer in sequential bits/blocks); a second buffer memory to store data (buffer 52 stores data; Fig. 4; 6/25-33), subsequent data area also stored in the data buffer sequentially (data stored in the buffer in sequential bits/blocks; 30/40-43); wherein the first and second buffer memories are integrated in and connected to the programmable memory (obviousness; see reasons in claim rejection; in re Larson); wherein the command and data written to the buffers are associated in their positions (level of associativity of the locations not indicated by applicant) (the data and command are written to their respective buffers, their locations; 6/15-54). The Examiner maintains that Norman teaches the invention, as presently claimed.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claim 1,5 recites the limitation "the accessed command" in multiple locations within the claim. There is insufficient antecedent basis for this limitation in the claim. Nowhere in the claim is there language for accessing a command. The only claim related language is "in the case of a program command access", which is interpreted as a mode of operation in which command can be accessed. This claim language does not mean that a command has been accessed/executed. Claim language clarification is required.

6. Claim 1,5 recites the limitation "the accessed data" in multiple locations within the claim. There is insufficient antecedent basis for this limitation in the claim. Nowhere in the claim is there language for accessing a command. The only claim related language is "in the case of a data access", which is interpreted as a mode of operation in which data can be accessed. This claim language does not mean that a data has been accessed/retrieved. Claim language clarification is required.

7. Claims 5-8 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. As to claim 5, Applicant claims (in preamble) "A method for performing at least one of a command access and data access". However, the claims step fail to include any step for perform a command or data access. Instead, the claimed steps only recite steps for storing command/data in the memory. As presently written, it is unclear as what is being claimed since the purpose of the claimed method does not correspond to the cited method steps.

8. Claims 2-4,6-8 are also rejected for incorporating the errors of the parent claim.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

10. Claims 1-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over by Norman et al (US 6,567,335).

As to claim 1:

11. Norman discloses a memory system having a memory controller connected to multiple memory devices. Norman discloses the claimed memory arrangement comprising: a programmable memory (flash memory 38; 4/48-67); a first buffer memory associated with the programmable memory, to which first buffer memory, in the case of a command access, at least one command following the accessed command is written (command buffer 48 stores/buffers commands going to command decode logic; Fig. 4; 3/5-12, 5/60-67; claim 29,32), subsequent command are also stored in the buffer sequentially (data stored in the buffer in sequential bits/blocks); and a second buffer memory to which, in the case of a data access, at least one datum following the accessed datum is written (data buffer 52 stores data from memory array; Fig. 4; 6/7-12, 13-20, 25-30; claim 29,32), subsequent data area also stored in the data buffer sequentially(data stored in the buffer in sequential bits/blocks; 30/40-43). The command and data written to the buffers are associated in their positions (level of associativity of the locations not indicated by applicant; the data and command are written to their respective buffers, their locations; Fig. 4; 5/56-6/20). Norman does not specifically teach the first buffer and

second buffer is integrated in the flash memory. The courts also have found that forming a single integral element from multiple elements would be a matter of obvious engineering choice and would be obvious one of ordinary skills in the art to save space and expense, with lower delays (In re Larson, 340 F.2d 965, 968, 144 USPQ 347, 349 (CCPA 1965). Thus, it would have been obvious to one of ordinary skills in the art at the time of the invention to integrate the first and second buffers in the flash memory of Norman to save space and expense.

As to claim 2:

12. Norman discloses the programmable memory includes a burst flash memory (flash memory 38; 4/48-67).

As to claim 3,7,8:

13. Norman teaches the second buffer memory is loaded only in the case of a data access (data input buffer 52 stores temporary data upon read; 6/7-12, 13-20,25-30; 8/40-50).

As to claim 4:

14. Norman teaches content of the first buffer memory (command input buffer 48-51) is not changed when the at least one datum is subsequently read from the second buffer memory (command buffer 48 and data buffer 52 not affected by one another (Figure 4).

As to claims 5-6:

15. Norman discloses a memory system having a memory controller connected to multiple memory devices. Norman discloses the claimed method for performing at least one of a command access and a data access during a program execution in connection

with a programmable memory, comprising the steps of: recognizing in the case of a command access that a command access is present; recognizing in the case of a data access that a data access is present; writing a command following the accessed command to a first buffer memory; and writing a datum following the accessed datum to a second buffer memory (command input buffer 48 stores/buffers commands going to command decode logic; Fig. 4; 3/5-12, 5/60-67; claim 29,32), data buffer 52 stores data from memory array; Fig. 4; 6/7-12, 13-20, 25-30; claim 29). Subsequent command/data are also stored in the command/data buffer sequentially (data stored in the buffer in sequential bits(blocks; 30/40-43)). The command and data written to the buffers are associated in their positions (level of associativity of the locations not indicated by applicant; the data and command are written to their respective buffers, their locations; Fig. 4; 5/56-6/20). It is well known in the art of memory design to integrate multiple devices onto a single chip to provide for faster access, smaller footprint/size, and reduced cost. The courts also have found that forming a single integral element from multiple elements would be a matter of obvious engineering choice and would be obvious one of ordinary skills in the art (In re Larson, 340 F.2d 965, 968, 144 USPQ 347, 349 (CCPA 1965)). Therefore, it would have been obvious to one of ordinary skills in the art at the time of the invention to integrate the first and second buffers in the flash memory of Norman.

Conclusion

16. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Than Nguyen whose telephone number is 571-272-4198. The examiner can normally be reached on 8am-3pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Than Nguyen
Examiner
Art Unit 2187